When are Transmission-Line Effects Important for On-Chip Interconnections?

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Abstract— Short, medium, and long on-chip interconnections having linewidths of 0.45–52 μm are analyzed in a five-metal-layer structure. We study capacitive coupling for short lines, inductive coupling for medium-length lines, inductance and resistance of the current return path in the power buses, and line resistive losses for the global wiring. Design guidelines and technology changes are proposed to achieve minimum delay and contain crosstalk for local and global wiring. Conditional expressions are given to determine when transmission-line effects are important for accurate delay and crosstalk prediction.

Index Terms— On-chip wiring, transmission lines.

I. INTRODUCTION

A S PROCESSOR cycle times become shorter and chips become larger and more complex, the performance of on-chip interconnections becomes more important. System integration on large dies transfers the package wiring on chip. Transmission-line properties of on-chip wiring need to be taken into account due to the long lengths and fast rise times encountered. The traditional lumped-circuit RC representation is no longer adequate, since it results in substantial underestimation of both crosstalk and delay. However, on-chip interconnects have unique characteristics, namely very high capacitive and inductive coupling and resistive losses, and very nonuniform transmission-line structures [1].

In this paper, we take a close look at the specific challenges of using short, medium, or long interconnections with linewidths from 0.45 to 52 μm. The relevance of transmission-line effects is explained, design guidelines are formulated for each category, and the performance-limiting parameters are highlighted. The short local wiring with the highest density are shown to be affected by the large capacitance and capacitive coupling to adjacent neighbors that generate excessive data-pattern-dependent delay and delay variation. The medium and long lines are mostly limited by the capacitive and inductive coupling, causing excessive crosstalk, especially when these lines are driven by larger devices (low-impedance drivers).

The delay on very long low-resistance lines strongly depends on the accurate prediction of both the resistance and inductance of the current return path in the power buses surrounding them. Examples will be given for each of these cases.

II. SHORT LOCAL WIRING

The majority of on-chip wiring is comprised of local circuit connections which have maximum lengths of 1–3 mm. Such lines use the minimum widths and spaces dictated by the technology. These lines are driven by small devices with a large effective impedance Z_{DRV} compared to the line Z_0. In such cases, the interconnects appear as lumped capacitive loads. As the circuit speeds increase, the interconnection delays start exceeding the logic block delays. The small wiring cross sections result in very high line resistance R. For frequencies $\omega = 2\pi/t_r$ for which $R \gg \omega L$

$$Z_0 \cong \frac{1-j}{\sqrt{2}} \sqrt{\frac{R}{\omega C}} \tag{1}$$

and most on-chip wiring is represented by RC circuits. For very short lines and slow devices, a single RC section has been generally used [2]. As the line lengths and circuit speeds increase (the wavelength decreases), distributed n-section RC representation has to be used for accurate delay predictions. The following approximate formula has been traditionally used for short lines [2]:

$$\mathrm{Delay} = Z_{\mathrm{DRV}} \cdot C_T + (Rl \cdot Cl)/2 \tag{2}$$

where C_T represents the total capacitive load seen by the driver circuit, which is approximated to have a constant impedance Z_{DRV} and $C_T = Cl + C_L$, or line capacitance plus load capacitance. Delay in (2) is the sum of gate delay and interconnect delay. In the case of short lines driven by small devices with large Z_{DRV}, the first term in (2) dominates. Moreover, the distributed RC-circuit representation assumed by (2) predicts a delay that increases in proportion to the square of the line length l. Short, very dense lines have very large capacitive coupling $K_C = C_{12}/C_{22}$ to adjacent wiring. This makes the delay data-pattern dependent. Depending on the direction of the voltage on the adjacent wiring, the effective capacitance of the line, Cl, will be either $Cl = C_{22} - 2C_{12}$ (for in-phase switching +++ pattern, with three adjacent symmetric lines $C_{12} = C_{23}$), $Cl = C_{22}$ (for no adjacent switching 0 + 0
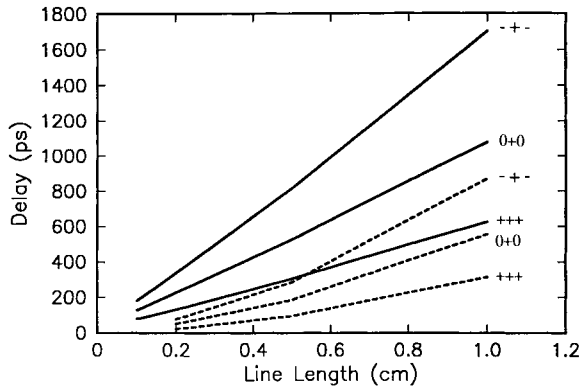
Fig. 1. Simulated propagated delay for three adjacent lines with width and space of 0.9 μm and $R = 494$ Ω/cm. Solid curves are for a 366-Ω driver circuit and the dashed curves are for a 50-Ω driver circuit. Each case has three curves for in-phase $(+++)$, out-of-phase $(-+-)$, and no-adjacent $(0 + 0)$ line switching.
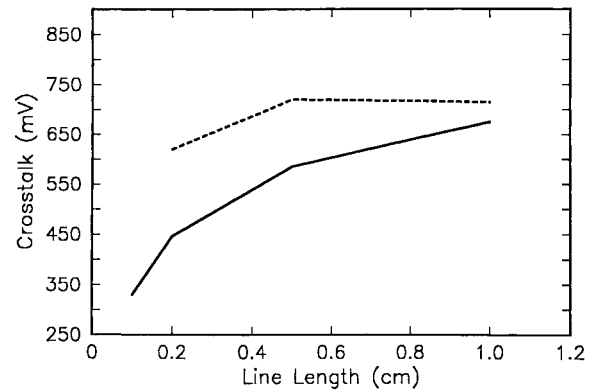

Fig. 2. Far-end crosstalk simulated for the lines of Fig. 1 with center line quiet and the other two switching in-phase. Active lines have input swing of 2.5 V and driver impedance of 50 Ω (dashed curve) and 366 Ω (solid curve).

pattern), or $Cl = C_{22} + 2C_{12}$ (for out-of-phase switching with $-+-$ pattern). The larger the capacitive coupling, the larger the delay variation on such interconnections.

An example is given in Fig. 1 for lines with 0.9-μm widths and spaces, 0.84-μm thickness, and built in a five-layer structure with AlCu metallization and SiO$_2$ insulator. The lines have resistance $R = 500$ Ω/cm, capacitance $C = 1.73$ pF/cm, and $K_C = 0.28$. The delay is plotted for lengths up to 10 mm and for two types of drivers with effective impedance of 50 and 366 Ω. The two driver circuits use devices with width-to-channel length ratios for the n-channel FET (NFET) of 220:1 and 30:1, respectively. The devices are built using CMOS technology with effective channel length $L_{\text{eff}} = 0.25$ μm and a 2.5-V swing. The data-pattern-dependent delay variation for 2-mm-long lines is $+49\%$, and -42% for a 366-Ω-driver and increases dramatically with length. For a 500-ps upper bound on interconnect delay, the maximum usable length $l_{\max}$ is only 3 mm for the smaller driving device, while it increases to 7 mm for the larger device. However, the smaller device is much more representative due to chip area and power limitations. In this case, the initial signal sent along the wiring is only $V_{\text{in}} = V_{DD}[Z_0/(Z_0 + Z_{\text{DRV}})] = 0.125$ V_{DD}, which means that several round trips are needed for the signal to approach the steady-state V_{DD} level. The rise-time at the end of a 2-mm line is 337 ps, while the driver signal has 60-ps transition. Even for a low-impedance driver circuit, the delay is increasing rapidly with length due to the very high resistive loss. The simulated results shown in Fig. 1 are based on distributed RLC-circuit representation. For the 0.9-μm-wide lines, the ratio $Rl/2Z_0$ is in the range of 0.5–4.7 for $l = 1$–10 mm, where $Z_0 = \sqrt{L/C} = 53$ Ω. It is shown in [3] that the voltage on a long, uniform, lossy transmission line excited by a unit step $u(t)$ can be expressed as

$$v(l,t) = [e^{-Rl/2Z_0} + B(l,t)]u(t - l\sqrt{LC}) \qquad (3)$$

where $B(l,t)$ is a slowly rising modified Bessel function [4]. For low resistance lines, Rl is small and the first term dominates. The line behaves like an LC circuit with fast-rising response. As Rl exceeds Z_0, the second term starts dominating, and the rise time is slowed down, similar to the

response of a slower RC circuit. The delay on such lines increases exponentially with length unlike the approximate prediction of (2).

However, in the case of the lines of Fig. 1 even for a low-impedance driver (Z_{DRV}), there will be very little difference in delay prediction when a distributed RC-circuit representation is used instead of the accurate distributed RLC approach. The waveforms predicted by an RC-circuit and a transmission-line treatment are different, but they will cross the switching threshold ($V_{DD}/2$) at very similar times because the slow resistive line behaves like an RC-circuit [3]. However, the faster signals obtained with the larger devices generate much higher crosstalk in proportion to $K_C + K_L$, but mostly K_C, as shown in Fig. 2. For a 20% noise budget (500 mV), for example, for the $Z_{\text{DRV}} = 50$ Ω, the maximum usable length drops to $l_{\max} = 1$ mm compared to the $l_{\max} = 7$ mm dictated by the maximum delay of 500 ps. The optimum design has to balance the need for fast signals with small delay, small delay variation, and short risetimes, with the containment of all the noise sources such as crosstalk, on-chip simultaneous switching noise, device switching threshold variation, and power supply tolerance. This is not the practice today. Performance-driven routers need to be developed that take into account several performance criteria simultaneously, not just delay.

III. SCALING OF LOCAL WIRING

The key parameters that limit the performance of short wiring are line capacitance C and capacitive coupling K_C. The 0.9-μm-wide lines with 0.9-μm-separations have $C = 1.73$ pF/cm and $K_C = 0.28$. The line and interlayer dielectric thicknesses are 0.84 and 1.2 μm, respectively. The width-to-thickness metal ratio is 1.07. The delay is 227 ps $+49\%$, -42% for $Z_{\text{DRV}} = 366$ Ω and $l = 2$ mm. Assume the linewidth and space are shrinking to 0.7 μm. This results in a width-to-thickness ratio of 0.83 and 22% increase in wiring density. K_C increases to 0.33 and $C = 1.85$ pF/cm due to the larger C_{12}. For a line length $l = 2$ mm, the delay increases to 239 ps, $+62\%$, -49%. The worst case delay increases by 15% (from 337 to 386 ps). It is difficult with the present fabrication techniques used for AlCu/SiO$_2$ material set to shrink the layer
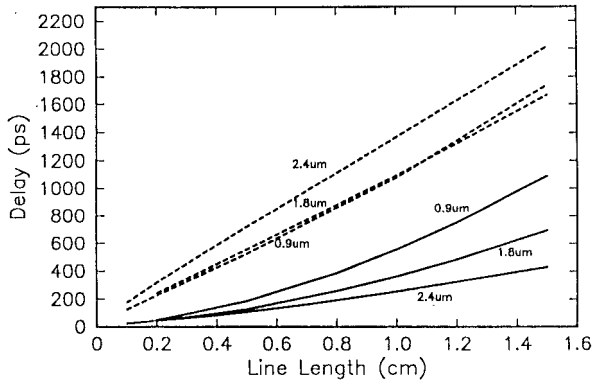
Fig. 3.   Simulated propagated delay for three adjacent lines on the third layer of a five-layer on-chip wiring stack with 0.9- and 1.8-μm widths and spaces, and 2.4-μm lines on the fifth layer for 50-Ω-impedance (solid curves) and 366-Ω-impedance (dashed curves) driver circuits. $R_{\rm dc} = 494$, 251, and 76 Ω/cm and $C = 1.73$, 1.85, and 2.6 pF/cm, respectively.

TABLE I

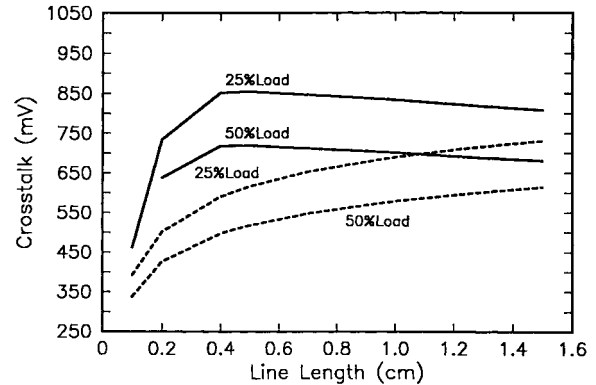| Maximum Useable Length			
w=0.9 um, s=0.9 um	Delay < 500 ps	Noise < 500 mV (20%)	Both
Zdrv=370 ohm	3 mm	3 mm	3 mm
Zdrv= 50 ohm	7 mm	1 mm	1 mm
w=1.8 um, s=0.9 um	Delay < 500 ps	Noise < 500 mV (20%)	Both
Zdrv=370 ohm	2.5 mm	4 mm	2.5 mm
Zdrv= 50 ohm	8 mm	1 mm	1 mm
w=1.8 um, s=1.8 um	Delay < 500 ps	Noise < 500 mV (20%)	Both
Zdrv=370 ohm	4 mm	no limit	4 mm
Zdrv= 50 ohm	10.5 mm	no limit	10.5 mm
w=2.7 um, s=3.6 um	Delay < 500 ps	Noise < 500 mV (20%)	Both
Zdrv < 125 ohm	16 mm	16 mm	16 mm

Fig. 4.   Simulated FEN for three adjacent lines with 1.8-μm widths and 0.9-μm spaces with either 50% or 25% orthogonal loading in the layers above and below. Simulations are for 2.5-V, 50-Ω (solid curves) or 366-Ω impedance (dashed curves) driver circuits. All cases have two active and one center quite line (+ 0 + data pattern).

thicknesses as the linewidths are reduced. The consequence is a scaling trend where the linewidth-to-thickness ratios are much less than unity. A 0.45-μm groundrule case, with thickness of 0.73- and 0.9-μm-thick dielectric, has $K_C = 0.36$ and width-to-thickness ratio of 0.62. Line capacitance is $C = 2.09$ pF/cm and delay variation is $+72\%$, -54%. Worst-case delay increases to 420 ps, which then drastically limits the maximum usable length.

In a five- or six-layer structure, there could also be significant vertical coupling between lines traveling in the same direction. This effect is especially strong when utilization of orthogonal channels is low, when lines on adjacent layers overlap (*wrong-way* routing) or when short lines couple to wider less resistive lines on upper layers that generate significant crosstalk, since signals propagate with faster risetimes along them.

In order to achieve higher wiring densities in the future, a following design guideline is useful for the short wires that have $R > 500$ Ω/cm. The goal should be to keep $C < 2$ pF/cm and $K_C < 0.30$. These restrictions imply technology improvements. Width-to-thickness conductor ratios close to unity (square cross section) require a fabrication technique that can generate thin metal and dielectric layers with small tolerances. K_C can also be lowered by lower dielectric-constant insulators used in the conductor layer. Overall lower dielectric-constant insulators lower C and, therefore, reduce delay and total chip power.

IV. MEDIUM-LENGTH LINES

In order to increase the maximum usable length, wider less resistive lines are used for medium-length interconnections. Table I and Fig. 3 show examples for lines with widths 2–2.7 times the minimum groundrule (0.9 μm), or 1.8 and 2.4 μm, that have $R < 250$ Ω/cm. The delay of wider lines with higher capacitance is larger because of the dominance of the first term in (2) when $Z_{\rm DRV} = 366$ Ω. Table I shows a maximum usable length limit of $l_{\rm max} = 2.5$ mm for the 1.8-μm-wide lines with 0.9-μm separation. Such lines are not adequately utilized unless lower impedance drivers $Z_{\rm DRV} = 50$ Ω, as

shown in Fig. 3, are used ($l_{\rm max} = 8$ mm for $Z_{\rm DRV} = 50$ Ω in Table I). The 2.4-μm-wide lines with $R = 76$ Ω/cm show the smallest delay for $Z_{\rm DRV} = 50$ Ω compared to the 1.8-μm-($R = 250$ Ω/cm) and 0.9-μm-wide lines ($R = 500$ Ω/cm). The improvement in delay afforded by the less resistive lines driven by larger devices with low-impedance $Z_{\rm DRV}$, however, has to be balanced against the allowable crosstalk budget. Fig. 4 shows the simulated crosstalk for the 1.8-μm-wide lines (0.9-μm separation) for two types of drivers and for 25% and 50% orthogonal loading cases. The increase in K_C from 0.25 to 0.29 results in higher noise. The small line-to-line separation of 0.9 μm, reduces $l_{\rm max}$ from 8 to 1 mm. $l_{\rm max}$, however, can be increased to 10.5 mm for a separation of 1.8 μm where $K_C = 0.11$ (Table I). Once the crosstalk limitation is eliminated, the resistive losses will dominate because the $Rl/2Z_0$ term in (3) becomes greater than unity and the second term begins to dominate.

It should be noted that in the case of the narrow lines with small separations, the capacitive coupling will not significantly change with orthogonal wiring utilization. For a 0.54-μm-wide line case, with 0.54-μm separation, 0.73- and 0.9-μm metal and dielectric thicknesses, respectively, K_C only changes from 0.38 to 0.33 for 0% and 50% loading (in layers above and below), respectively. For wider lines and separations, the loading has larger impact. For 0.8-μm widths and separations,
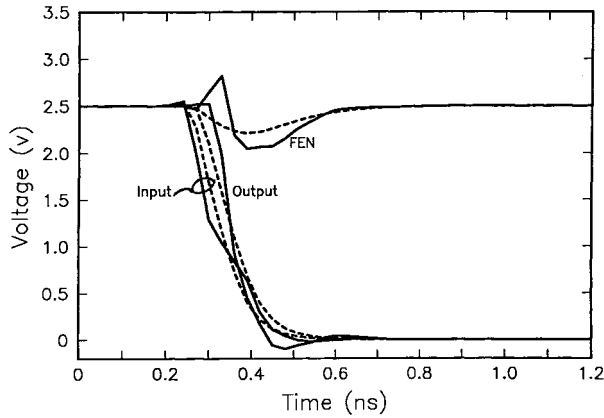
Fig. 5. Simulated propagated waveforms and far-end crosstalk FEN for 2.4-μm-wide lines with 2.4-μm spaces with $R = 76$ Ω/cm, $l = 5$ mm, and for 50-Ω impedance driver circuit. The FEN noise is obtained for two active and center quiet line and 2.5-V input signal swing. Simulations were performed with either distributed RLC (solid curves) or distributed RC circuit representation (dashed curves).

Fig. 6. Simulated FEN for three adjacent lines with 2.4-μm width and 2.4-μm spaces (same as in Fig. 5). Simulations are for 2.5-V, 50-Ω (solid curves) or 366-Ω impedance (dashed curves) driver circuits; either with distributed RLC or distributed RC circuit representation. All cases have two active and one center quite line ($+$ 0 $+$ data pattern).

dielectric height of 0.8 μm, and metal thickness of 0.5 μm, for example, K_C changes from 0.32 to 0.20 for 0% and 50% loading, respectively.

Fig. 5 shows the signal propagation and crosstalk for a 5-mm-long line ($R = 76$ Ω/cm), which has 2.4-μm width and spacing and 2.1-μm thickness. The initial signal transition is much faster than the more rounded slower part of the falling edge. The LC-like circuit behavior predicted by (3) is present at the beginning of the transition, before the RC-like behavior takes over. The faster LC part will also generate higher crosstalk, which is not predicted adequately by a distributed RC circuit. The far-end-noise (FEN) monitored at the end of the quiet line, far from the driver, has a positive peak higher than 2.5 V, which is proportional to the difference $K_C - K_L$ [3] and is not present for the RC simulation that omits inductive coupling. The width is proportional to the initial fast transition. The negative peak, lower than 2.5 V, is due to the reflected noise from the near-end of the quiet line, is wider, and is proportional to $K_C + K_L$, but is primarily determined by the K_C contribution. This is the backward traveling noise [3]. Fig. 6 plots the discrepancy in crosstalk prediction when inductive coupling is not taken into account. Note in Fig. 5 that both distributed RLC and RC representations predict similar delays. The input signal at the driver end shows large discrepancies in waveforms because a transmission-line representation is accounting for the effective Thevenin equivalent-circuit signal generation predicted by the ratio $Z_0/Z_{\text{DRV}} + Z_0$, which is not considered by the RC circuit. The output waveforms, although different in shape, cross the $V_{DD}/2$ threshold at similar times. The width of the reflected noise from the near-end of the line is proportional to twice the propagation delay on the line and the time constant of the RC circuit formed by the line impedance, the driver impedance, and the load. In Fig. 5, the noise returns to the steady-state level of 2.5 V after about 400 ps. Such wider noise signals have a higher probability of overlapping with other noise sources in the incident-switching time window. By contrast, the narrow initial noise pulse will not be fully
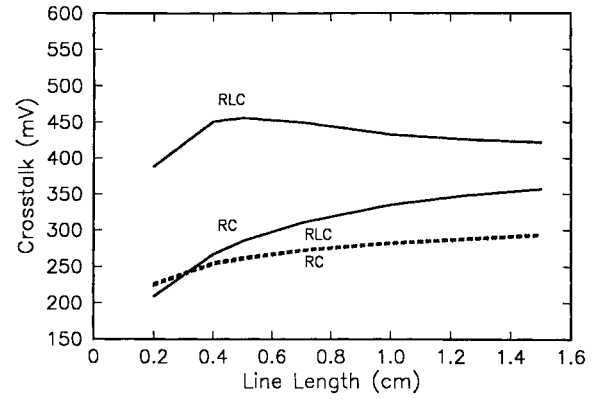
detected by a receiver circuit, and its effect on noise budget depends on the bandwidth of the receiver device.

The wider lines that have lower resistance ($R < 250$ Ω) can propagate fast signals on longer lengths when driven by low-impedance drivers. They should have proportionally larger line-to-line separations (separation should be larger than the insulator thickness $S > H$) that result in lower crosstalk. Such lines would also benefit from somewhat thicker interlayer insulators, as was recommended in [5]. We recommend to control K_C such that $K_C \leq 0.15$–0.20. For the examples given with $W = 1.8$ μm, $S = 0.9$ μm, $W = S = 1.8$ μm, and $W = S = 2.4$ μm, K_C is 0.23, 0.11, and 0.15, respectively, and K_L is 0.65, 0.32, and 0.54. Inductive coupling should be taken into account to avoid noise underestimation.

V. LONG LINES

Long lines fall primarily in three categories: data-buses, control, or clock. Control lines could exceed one-chip-edge in length, travel alone, but could have large fan-outs. Data lines between central processing unit (CPU) and cache travel in groups, generally have half-a-chip-edge in length, and have a small load at the receiver. Such lines synchronously operate and are designed for minimum path delay over fairly long lengths. They represent a small fraction of the total number of on-chip nets and, therefore, can be placed on the thicker topmost layers. They share real estate with the very wide power buses. Due to their synchronous and possible in-phase data pattern, line-to-line separation is generally designed to ensure containment of crosstalk. We recommend to have $S > W$ and to keep $K_C < 0.15$. Most often, the top metal layer is not planarized to reduce fabrication cost. The undulatory topography results in large variation of the linewidths and can increase line capacitance when compared with a planar process (such increase was shown to be as large as 35% [1]). Once again, such lines benefit from the use of thicker interlayer insulators as highlighted in Fig. 7. 2.7- and 6.3-μm-wide lines are driven by devices having an effective impedance of 11–275 Ω for $l = 8.5$ mm. The wider line has lower resistance ($R = 25$ and 55 Ω/cm for the $W = 6.3$
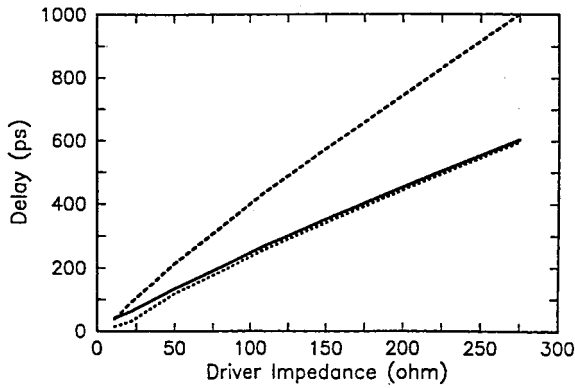
Fig. 7. Simulated propagated delay for lines with 2.7-μm width, 3.6-μm-space, and insulator thickness of H = 0.9-μm (solid curve), 6.3-μm-wide, with 8.1-μm space, H = 0.9-μm (dashed curve), and for W = 2.7 μm, S = 3.6 μm, and H = 2.1 μm (dotted curve). Line resistance is R = 55, 25, 25 Ω/cm, capacitance is C = 1.7, 2.9, and 1.7 pF/cm, and line impedance is Z_0 = 37, 23, and 36 Ω, respectively, for the three designs. All lines have l = 8.5 mm and driver circuits have 11–275-Ω impedance.

Fig. 9. Simulated FEN for 4.8-μm-wide line on top of 2.7-μm-wide line two layers below. There is 50% orthogonal wiring in the adjacent layer and l = 1.6 cm. The lines have R = 35.5 and 167.8 Ω/cm, C = 4.18 and 1.74 pF/cm, Z_0 = 38.5 and 62.7 Ω, and K_C = 0.08 and 0.21, and K_L = 0.73 and 0.67, respectively for the two lines. The wide line is driven by a 50-Ω impedance device with 2.5-V swing. Simulations were performed with frequency-dependent ($RLC(f)$) (solid curve), frequency-independent RLC (dashed curve), and RC circuit representations (dotted curve).

While such wide lines on a top layer are designed with wide separations for intralayer crosstalk containment, the distance to layers underneath is relatively small and can result in substantial vertical coupling. Fig. 9 shows such an example of parallel 4.8- and 2.7-μm-wide lines on the topmost layer and two layers below, respectively. The crosstalk is shown to be less that the 500-mV maximum budget for $l < 8$ mm. The line on the top layer is driven by a low-impedance 50-Ω driver, which will make possible the propagation of very fast signals. Once again, the distributed RLC-circuit representation which accounts for both capacitance and inductive coupling is essential for correctly estimating the crosstalk.

Clock lines are single lines with cluster configuration. They start from centrally located buffers and have branches of the cluster extend to the edges of the chip. Each branch can be about half-a-chip-edge in length. A clock driver typically drives several such branches with equal delay for all positions on the chip. Each branch, whether a tree or grid layout, has a very large number of fan-out loads. Clock lines may drive thousands of circuits per branch, which means the feeding branch has to have a lower Z_0 than the equivalent fan-out connections in order to provide first incidence switching. The driver circuit size is quite large in order to have $Z_{\mathrm{DRV}} < Z_0$ and tapered Z_0 line segments are sometimes used in tree structures. Grids rely on duplication of many drivers. The critical design issues are controlled cross section across the chip, low resistance, low capacitance or high Z_0, and isolation from other signal lines. Clock lines can generate unwanted in-plane and interplane crosstalk and common-mode noise. The reference current return path may be custom designed in order to control line characteristics and the return-path resistance should be a small fraction of total line resistance. Based on extensive analysis, we recommended to design these lines such that the return-path effective resistance is less than one quarter of the total effective resistance. Such a guideline is independent of the technology used. Using thick layers without correspondingly thick insulators results in very high-capacitance (low-Z_0) lines that propagate slow signals and are
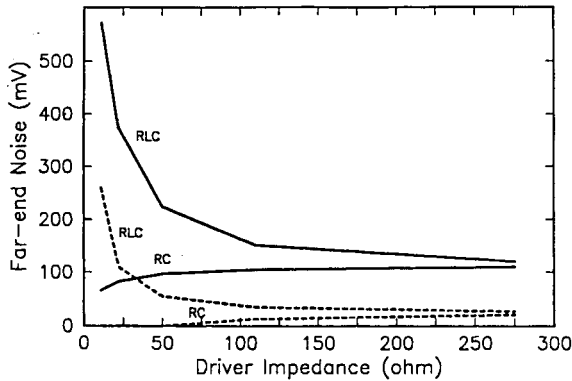

Fig. 8. Simulated FEN for the lines of Fig. 7 with 2.7-μm width (solid curves) or 6.3-μm width (dashed curves). Simulations were performed with either distributed RLC or distributed RC circuit representation and 2.5-V-swing driver circuits.

and 2.7 μm, respectively) but the capacitance is higher by a factor of 2.5 compared to the narrow line case. The line impedance is then too low, or the capacitive load on the driver is too high [as seen from (2)] and the more resistive lines can propagate faster signals. The 6.3-μm-wide line is also modeled on top of a 2.1-μm-thick insulator, which then results in much lower delay with its capacitance being equal to that of the 2.7-μm line above a 0.9-μm-thick layer. The delays are very similar in this case. The 2.7-μm-wide lines with 3.6-μm separation (K_C = 0.06) can be used up to 16 mm with $Z_{\mathrm{DRV}} < 125$ Ω for a maximum delay of 500 ps (Table I). Once again, the faster signals obtained with larger size driver circuits generate larger crosstalk on adjacent quiet lines. Fig. 8 plots the crosstalk at the far end of the quiet line for the 2.7- and 6.3-μm-wide lines of Fig. 7 when distributed RLC and RC circuit representations are used. The discrepancy in crosstalk prediction is most significant for the low-impedance driver cases. In these simulations, both the active and quiet lines are driven by the same size devices and small loads are assumed at the receiver end.
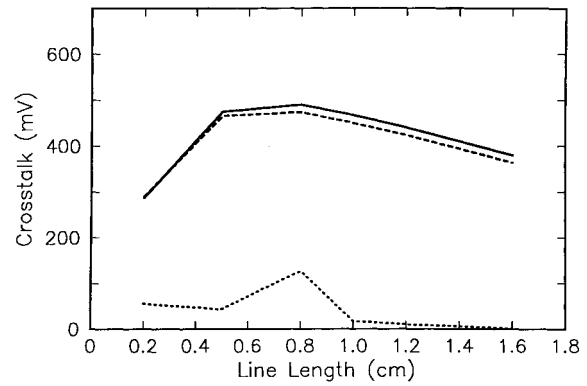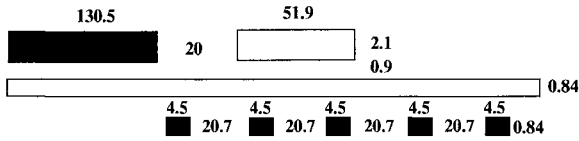
Fig. 10. Cross section for 51.9-μm-wide line on topmost layer with 20-μm distance to wide power bus. 4.5-μm-wide power buses are shown two layers below. There is 50% orthogonal wiring loading on layer below. $R = 8.0$ Ω/cm ($R_{\mathrm{dc}} = 3.5$ Ω/cm), $C = 27.3$ pF/cm, and $Z_0 = 8$ Ω. Calculations were performed with a three-dimensional (3-D) full-wave parameter extractor [6].

TABLE II

Width=29.4 um

Rtot = 63 ohm/cm, Zo=10 ohm, C = 15.5 pF/cm, Rdc = 18.5 ohm/cm

	R(f)L(f)C	Δ	RLC	Δ	R_{TOT}C	Δ	RdcC
Delay (ps)	217	-9%	203	-2%	213	-37%	136
Risetime (ps)	335		354		413		248

Width=7.5 um

Rtot = 35 ohm/cm, Zo=28 ohm, C = 4.8 pF/cm, Rdc = 24.4 ohm/cm

	R(f)L(f)C	Δ	RLC	Δ	R_{TOT}C	Δ	RdcC
Delay (ps)	92	-16%	77	-33%	62	-42%	53
Risetime (ps)	111		68		163		130

hard to drive. Slow signals also have larger delay variation, thus adding to clock skew.

Fig. 10 shows a typical clock wiring design placed in the uppermost metal layer. The line is 51.9-μm wide, has $R_{\mathrm{DC}} = 3.5$ Ω/cm, $Z_0 = 7.6$ Ω, and $C = 27.3$ pF/cm. It is placed 20-μm away from the low resistance current return reference bus (130.5-μm wide). The line Z_0 will then depend quite strongly on the presence of the narrow power buses (4.5-μm wide) on the layers underneath, since they are much closer to the clock line than the 130.5-μm-wide current return bus. The absence of the two power buses underneath the line would increase the inductance by a factor of two. However, it is also important to realize that the return-path resistance is quite high in this case. The narrow power buses have much higher resistance than the line resistance, unlike the case for the narrower lines discussed in the previous sections. Typical power bus widths are 2.7–4.5 μm, with metal thickness around 0.84 μm and $R = 99$–165 Ω/cm. The effective line resistance R is twice the R_{DC} of the signal line, $R = 7.5$ Ω/cm for the example shown in Fig. 10 with $R_{\mathrm{DC}} = 3.5$ Ω/cm for the signal line. Signal propagation on these clock lines is shown using both a distributed RC-circuit and an RLC-circuit representation. For the RC circuit, two cases are considered: with, (($R_{\mathrm{DC}} + R_{\mathrm{GND}})C$), and without, ($R_{\mathrm{DC}}C$), the contribution of the return-path resistance. RLC-circuit representation is calculated with ($RLC(f)$) or without, (RLC) frequency-dependent parameters. For the $RLC(f)$ case, the $R(f)$ and $L(f)$ is used over the entire frequency range dc −10 GHz. Table II shows the results for $l = 5$-mm-long lines driven by an 11-Ω-impedance driver cir-
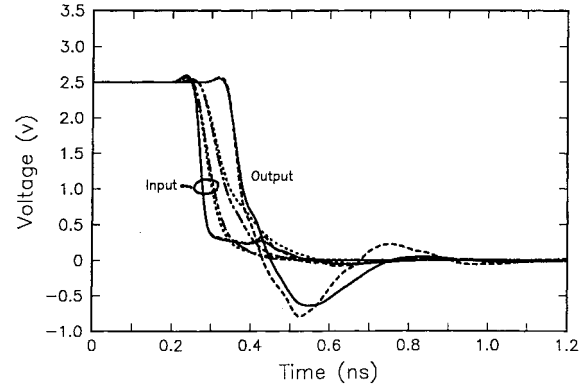

Fig. 11. Simulated propagated waveforms for 7.5-μm-wide line that is 2.4-μm away from a wide power bus on topmost layer, with $R = 35$ Ω/cm, $C = 4.8$ pF/cm, and $Z_0 = 28$ Ω (shown in Table II). Simulations are shown for 11-Ω impedance driver, $l = 5$ mm, and with $RLC(f)$ (solid), RLC (dash), ($R_{\mathrm{dc}} + R_{\mathrm{GND}}$) C (dot), and (R_{dc} C) (dot–dash) circuit representations.

cuit for 29.4- and 7.5-μm-wide lines. The distributed $R_{\mathrm{DC}}C$ (50 subsections) representation underestimates path delay by 37%–42% compared to the accurate $RLC(f)$ representation. The ($R_{\mathrm{DC}} + R_{\mathrm{GND}}$)$C$ or $R_{\mathrm{TOT}}C$ circuit is quite close to the exact simulation and so is the RLC circuit for the wider slower line. This indicates the importance of including and controlling the return-path resistance. It can be seen that the wider lines are fairly resistive, with $Rl/2Z_0 = 1.6$ and unable to propagate extremely fast signals even when driven by very low-impedance drivers. Once again, the signal on the narrower 7.5-μm-wide lines, with lower C and higher Z_0 is faster than on less resistive lines that are wide ($W = 29.4$ μm) and have $Z_0 < Z_{\mathrm{DRV}}$ and large C_T. The 7.5-μm-wide has $Rl/2Z_0 = 0.4$ and propagates much faster signals. In this case, the inductance needs to be taken into account as well. Fig. 11 shows the simulated waveforms for the line with $W = 7.5$ μm. These lines show very typical LC-type of behavior. Fig. 12 shows the very slow signal propagation and multiple reflections caused by the small value of the ratio $Z_0/(Z_0 + Z_{\mathrm{DRV}})$ for the 51.9-μm-wide lines. The wider lines have large capacitance, impedance lower than Z_{DRV}, and transmit slow RC-like signals.

VI. Guidelines for Transmission-Line Effect Consideration

Table III summarizes the characteristics of the short, medium, and long lines discussed in the previous sections. The ($Z_{\mathrm{DRV}} \cdot C_T$) and [($Rl \cdot Cl$)/2] terms of (2) and the ($Rl/2Z_0$) of (3) are also calculated. The wave-propagation delay can be approximated by Z_0Cl or $\tau l \cong \sqrt{LCl}$. In a general case, Z_0, L, and C can all be frequency-dependent. Further, τ is not a constant, but increases along a resistive line, and when the line delay is shorter than the propagated risetime, several round-trip delays are needed before the signal reaches steady-state levels and full transition. In Table III, we assume that Z_0Cl is a constant depending only on line length. In addition, $C_L \ll Cl$ (load is small) and $C_T \cong Cl$. In all cases, R includes the current return-path resistance in the power buses. All the examples are shown for lines of the

TABLE III
NECESSARY CONDITIONS FOR RLC MODELING OF DELAY AND CROSSTALK

Zdrv = 50 Ω, Vdd = 2.5 V, l = 5 mm

Line width (μm)	R (Ω/cm)	L (nH/cm)	C (pF/cm)	Zo (Ω)	$\frac{Rl}{2Zo}$	$ZdrvC_T$ (ps)	$1/2\,RCl^2$ (ps)	ZoCl (ps)	Del. RLC (ps)	Δ	Del. RC (ps)	FEN RLC (mV)	Δ	FEN RC (mV)
0.9	494	4.75	1.73	52	2.4	43	107	45	186	0	186	720	-10%	648
1.8	248	3.70	1.85	45	1.4	46	58	42	129	0	129	270	-17%	225
2.4	76	5.30	2.60	45	0.4	65	25	59	103	+6%	109	500	-42%	288

Zdrv = 11 Ω, Vdd = 2.5 V, l = 5 mm

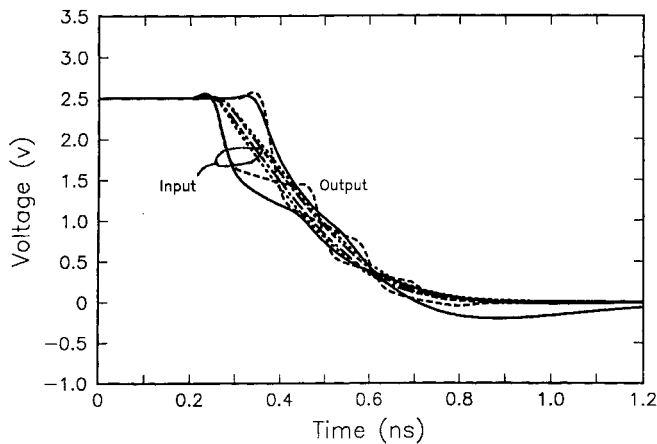| Line width (μm)	R (Ω/cm)	L (nH/cm)	C (pF/cm)	Zo (Ω)	$\frac{Rl}{2Zo}$	$ZdrvC_T$ (ps)	$1/2\,RCl^2$ (ps)	ZoCl (ps)	Del. RLC (ps)	Δ	Del. RC (ps)
7.5	35	3.47	5.16	26	0.4	27	23	67	89	-27%	65
51.9	8	1.60	27.3	8	0.3	150	26	109	213	-5%	203

Fig. 12. Simulated propagated waveforms for the 51.9-μm-wide line shown in Fig. 10. Simulations are shown for 11-Ω impedance driver, $l = 5$ mm, and with $RLC(f)$ (solid), RLC (dash), $(R_{dc} + R_{GND})\,C$ (dot), and $(R_{dc}\,C)$ (dot–dash) circuit representations.

same length of 5 mm. The lines with 0.9-, 1.8-, and 2.4-μm widths are driven by 50-Ω-impedance driver circuit, while the lines with $W = 7.5$–51.9 μm have $Z_{DRV} = 11$ Ω. These Z_{DRV} values are considered representative of actual use.

A. Delay Prediction Dependence on Inductance

We formulate a guideline to suggest when inductance is important for accurate delay prediction. In order to transmit fast signals that have LC-like behavior, the $(Rl/2Z_0) < 1$ condition from (3) needs to be satisfied. This implies small resistive losses. However, in addition, the equivalent driver impedance should be less than the line impedance $(Z_{DRV} < Z_0)$ in order to inject most of the available energy into the line. This is equivalent to requiring that the gate delay $Z_{DRV}C_T$ be less than the interconnect delay, which can be approximated by $1/2RCl^2$ from (2) for shorter lines. This condition corresponds to the dominance of the second term in (2). We, therefore, require the gate delay to be less than the RC delay of the line and less than the wave-propagation delay. This condition then becomes $Z_{DRV}C_T \cong Z_{DRV}Cl < 1/2RlCl < Z_0Cl$

or $Z_{DRV} < Z_0$. The faster the propagated signal, the larger the discrepancy in delay prediction between RC and RLC simulation. If the following conditions are met:

$$C_L \ll Cl \tag{4a}$$

$$Rl/2Z_0 \leq 1 \tag{4b}$$

$$Z_{DRV} < nZ_0 \tag{4c}$$

with

$$n = 0.5 - 1 \tag{4d}$$

then the error in prediction between RC and RLC representation will exceed 15%. The acceptable error limit will affect the limits defined in (4b) and (4d).

In Table III, the $Rl/2Z_0 \leq 1$ condition is only satisfied for lines with $R < 76$ Ω/cm. If, however, this is achieved only by widening of the signal conductors, C increases rapidly and the $Z_{DRV} \cdot C_T < Z_0Cl$ condition is no longer valid. The signal propagation is slowed down as in the case of $W = 51.9$ μm. Such lines need thicker insulator layers to reduce C and thus have higher Z_0. The difference in delay prediction is small for the wide lines in Table III. Only the 7.5-μm-wide line with $Z_0 = 26$ Ω, and $R = 35$ Ω shows a large delay prediction error.

B. Crosstalk Prediction

The waveforms in Fig. 5 highlight the initial fast LC-like transition of the signals even for fairly resistive lines. This fast transition will generate additional crosstalk which is not accounted for by capacitive coupling alone. The RLC matrices have to be used in the crosstalk simulation. Table III also compares the crosstalk prediction difference for RC-circuit compared to RLC-circuit representations. Even when delay prediction difference is small, the crosstalk discrepancy could be large. We formulate the following condition for when inductive coupling has to be taken into account in order for crosstalk prediction difference to be greater than 20% between

RC and RLC modeling:

$$C_L \ll Cl \tag{5a}$$

$$Rl/2Z_0 \leq 1.5 \tag{5b}$$

$$Z_{\text{DRV}} < nZ_0 \tag{5c}$$

with

$$n \cong 1 - 1.5 \tag{5d}$$

These conditions imply that the lines can be quite resistive and the driver size can be fairly small for inductive coupling to generate substantial additional crosstalk. In fact, the crosstalk difference can exceed the 20% limit even for 0.9-μm-wide lines ($R = 500$ Ω/cm), but only for lines $l < 3$ mm (not shown in Table III) when $Z_{\text{DRV}} = 50$ Ω. While this is a large discrepancy, it is unlikely that the very narrow, 0.9-μm-wide lines would be driven by such low-impedance drivers in practical applications due to the large crosstalk shown earlier in Fig. 2. Therefore, inductive coupling becomes relevant for wider lines, with $W > 1.8$ μm, or $R < 250$ Ω/cm.

When such lines are driven by devices with $Z_{\text{DRV}} \leq Z_0$, the noise increases with length for shorter lines and then slowly decreases as seen in Figs. 4, 6, and 9. The shorter lines transmit the faster signals that generate larger noise. As the active signal slows down on longer lines and resistive attenuation is larger, the crosstalk decreases. The noise amplitude will be a function of $K_C - K_L$ or $K_C + K_L$ and the incident wave amplitude or the ratio $[(Z_0/(Z_0 + Z_{\text{DRV}})]V_{\text{in}}$. For $Z_{\text{DRV}} > Z_0$, the noise increases monotonically with length as seen in Figs. 4 and 6 and will be a wide pulse that stays on for a large fraction of the cycle time. The incident signal reaches steady state very slowly and the time constant for the noise to return to steady-state level is large. Such lines exhibit only noise which is in the same direction with the switching transition on the active line (backward traveling noise). The narrow pulse-shaped forward-traveling noise [3] is not present or very small. In all these cases, the active and quiet lines are driven by the same size devices, and peak noise is reported. Bandwidth limitations of various receiver circuits will affect the limits defined in (5b) and (5d).

VII. SUMMARY AND CONCLUSIONS

The performance limiting parameters have been highlighted for short ($R > 500$ Ω/cm), medium ($R < 500$ Ω/cm), and long lines ($R < 100$ Ω/cm). Guidelines have been formulated for when inductive effects are significant both for delay and crosstalk prediction, and design recommendations were also given for each category. The conclusions are as follows. The short local wiring with the highest density and $R > 500$ Ω/cm are found useful for lengths less than 3 mm. As the scaling to smaller dimensions continues, the short wires will have resistance several times this value, but their behavior will stay the same. Their capacitance and capacitive coupling to adjacent neighbors are the limiting factors due to delay and delay variation. Such lines could benefit from lower in-plane dielectric-constant insulators, processes that allow close to a square (rather than tall) rectangular cross sections, and thinner

interlayer insulators. Even a transition from SiO$_2$ with $\epsilon_r = 4$ to a polymer with $\epsilon_r = 3$ translates into up to 25% performance improvement. The line-to-line capacitive coupling with the present approach of small width-to-thickness ratios renders these lines unscalable to smaller wiring pitches due to excessive data-pattern-dependent-delay variation. Future designs need to maintain $C < 2$ pF/cm and $K_C < 0.30$.

The medium-length lines with $100 < R < 500$ Ω/cm can be used for lengths up to 10 mm if driven by low-impedance drivers and have wide line-to-line separations that result in low crosstalk ($S > H$). This is especially important as noise budgets are shrinking. Smaller devices use lower V_{DD} levels that could generate lower noise. However, signal transitions are faster, thus resulting in higher noise. In addition, processing tolerances for both the devices and interconnect layers, and larger V_{DD} variation result in overall noise budget reduction. Noise sources also have a higher probability of overlapping within the shorter cycle-time windows. Such lines need medium-thickness insulators [5], lower resistivity metallization such as copper, and inductive coupling has to be taken into account to avoid noise underestimation. Based on our analysis we recommend to keep $K_C < 0.15$–0.20. This ensures that the main noise contribution which is proportional to K_C is not excessive. The additional noise generated by the K_L term can then be minimized by providing a rich supply of power/ground buses. Once the crosstalk limitation is eliminated, the maximum usable length is only determined by resistive losses.

The longer lines, such as data-buses, control, and clock lines, with $R < 100$ Ω/cm, can propagate fast signals for lengths greater than 10 mm. Such lines need thick planar insulator layers to increase Z_0 and reduce delay, wide line-to-line separations ($S > W$) to reduce crosstalk, and low resistivity metallization to reduce resistive losses both in the line and the power buses surrounding them. RLC-circuit representation is necessary for both delay and crosstalk. In this paper, we recommend to keep $K_C < 0.15$. The control of the current return path in the reference buses is shown to be essential for minimizing clock skew and to ensure controlled-impedance transmission-line behavior. Vertical coupling needs to be carefully assessed, especially for these wider lines, and could be alleviated by the use of shielded structures. It is also important to monitor the rise and fall time dispersion at the receiver input. As the cycle times become narrower, slower transitions cannot be tolerated because they could reduce the steady-state logic levels and thus the noise margin. In addition, slow transitions increase the variation in the receiver switching time and thus increase cycle time. Such transitions have to be restricted to being less one third to one half the cycle time.

Present-day routers have delay as the only restriction. Performance-driven routers with built-in fast simulators that optimize driver size for the given loads before routing will become essential for the many hundreds of megahertz clock microprocessor chips. The performance parameters are delay, delay variation as a function of adjacent switching activity, propagated transitions at the receiver input, and crosstalk. Such routers can rely on either a database of wiring rules or have a very fast coupled-line simulator as a front end to the tool for estimation before routing. Both approaches require

very powerful 3-D RLC-line parameter extractors for the hundreds of thousands of on-chip wiring nets.

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